

# DESIGN *FAQs*

## Frequently Asked Questions:

### POWER OVER ETHERNET

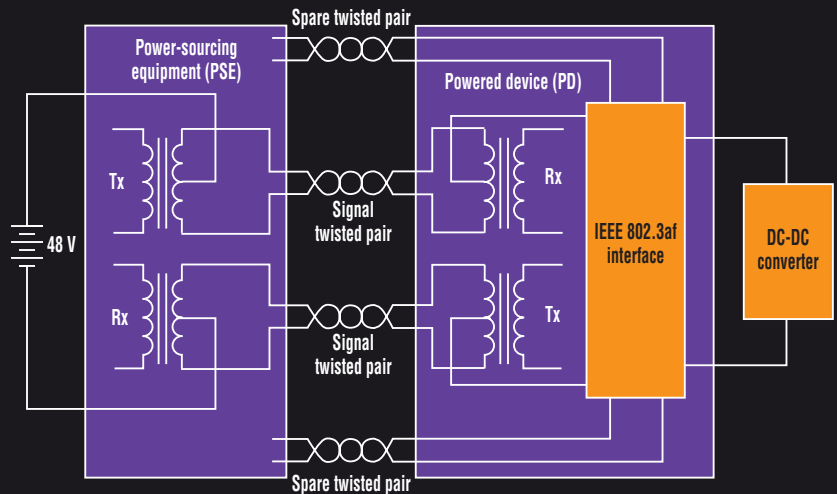
Sam Davis, Contributing Editor

#### What is the basis for Power over Ethernet (PoE)?

The IEEE 802.3af standard for PoE enables all data-terminal equipment (DTE) to receive power over the same cabling used for data. It specifies the protocol for delivery of 48 V dc over unshielded twisted-pair cables, such as Category 5. This eliminates the need for local power sources.

#### What does IEEE 802.3af cover?

The IEEE 802.3af standard presents the requirements for providing and receiving power over existing cabling. It involves power-sourcing equipment (PSE), which provides the power on the cable, and the powered device (PD), which receives the power. This standard defines the interface between the PSE and PD as it relates to the associated detection and classification protocol. The figure shows a simplified typical PoE system.



The PoE system employs spare twisted-pair cables that are available in an Ethernet configuration. The dc-dc converter may be an external device. Or, it may be integrated partially or totally within the monolithic PoE IC.

#### How does the PoE System know when power is required?

A PD requests power with a detection algorithm that asks the PSE to look for a valid PD. The PSE looks for a valid PD by sending out 2.8 to 10 V across the power lines. A valid PD detects this voltage and places a resistance of 23.75 to 26.25 k $\Omega$  across the power lines. Upon detection of the resulting current, the PSE concludes that a valid PD is requesting power.

#### What does the PD do if it cannot accept power?

If the PD cannot accept power, it places a resistance above or below the values listed for a valid PD. On the lower end, a 12- to 23.75-k $\Omega$  range signifies that the PD doesn't require power. On the higher end, the range spans 26.25 to 45 k $\Omega$ . The PSE interprets any resistance less than 12 k $\Omega$  and greater than 45 k $\Omega$  as an invalid PD detection signature.

#### What are the power and current limitations in a PoE system?

The maximum current delivered to a node is 350 mA. Accounting for some power loss in the associated cables, the total amount of continuous power delivered to each node is 12.95 W.

Sponsored by National Semiconductor Corp.

#### How does the PSE determine the necessary power requirements?

After the detection phase, the PSE can optionally initiate a classification of the PD. The PSE uses the PD's classification to determine the maximum power required by the PD during normal operation. The IEEE 802.3af standard defines five different levels of classification that cover minimum and maximum power and voltage.

#### How does the PSE determine the classification?

The PSE increases the voltage across the power lines to between

15.5 and 20.5 V. The amount of current drawn by the PD determines the classification.

#### What does the PSE do next?

After finishing the detection and optional classification phases, the PSE ramps its output voltage above 42 V. Upon reaching the undervoltage-lockout (UVLO) release threshold, an internal FET turns on, and the PD begins to operate normally. It continues to do so as long as the input voltage remains above the UVLO threshold. For most PDs, an on-board dc-dc converter downconverts the input voltage and generates the required voltages.

#### What is the effect of capacitance?

# PRODUCT Q&As

## INTEGRATED POWER-OVER-ETHERNET PD INTERFACE AND PWM CONTROLLER

National's new LM5070 PoE PD device provides the highest integration, utmost reliability, and most versatile programmability available on the market today. Providing a minimum component solution for powered devices (PDs) in IEEE 802.3af Power-over-Ethernet (PoE) systems, the LM5070 includes the appropriate interface, hot-swap controller, and pulse-width modulation (PWM) dc-dc controller, integrated into one monolithic IC.

The LM5070's fully compliant interface includes signature detection, classification programming, and programmable undervoltage lockout (UVLO). The programmable UVLO features independently programmable hysteresis via a switched internal 10- $\mu$ A current source that forces additional current into the external resistor divider. Connecting the UVLO resistor divider directly across the input terminals will limit programmability and may even cause the system to violate 802.3af requirements. The LM5070 solves this issue by providing a current return pin for the divider called UVLORTN. The bottom resistor of the divider is connected to UVLORTN instead of tying it directly to the system return (-48 V).

The LM5070's hot-swap section includes an 80-V, 1- $\mu$ s, 400-mA internal MOSFET switch and associated control. Inrush currents lower than 400 mA may be required, as some legacy power-sourcing equipment (PSE) systems aren't capable of supplying full power (15 W). The LM5070 allows single-resistor programming of the inrush current level, and this same circuitry provides dc current-limit protection during normal operation.

The LM5070's PWM controller includes current limit, voltage reference, error amplifier, slope compensation, and soft-start. This high-speed biCMOS IC has total propagation delays less than 100 ns and a 1-MHz capable oscillator programmed by a single external resistor. The PWM controller enables all the advantages of current-mode control, including line feed-forward, cycle-by-cycle current limit, and simplified loop compensation. An internal gate driver can source and sink peak currents of 800 mA for an external power MOSFET operating in either a forward or fly-back configuration. The IC also has a high-voltage startup bias regulator (VCC) that operates up to 75 V and can be elevated by an auxiliary winding to improve system efficiency. Two options are available, providing either 80% maximum duty cycle limit with slope compensation (-80 suffix) or 50% maximum duty cycle without slope compensation (-50 suffix).



According to the IEEE 802.3af specification, if the input capacitance is less than 180  $\mu$ F, the PSE must limit the inrush current. An input capacitance greater than 180  $\mu$ F requires the PD to limit the inrush current to less than 400 mA. The PD must also present an input capacitance between 0.05 and 0.12  $\mu$ F to the PSE.

### How does the PoE handle transients?

The use of long cable lengths and transformers may result in over 68-V transients. To prevent these transients from exceeding the application's maximum voltage, designers can place a transient voltage surge suppressor (TVS) or similar zener type device between the positive input supply and the negative input supply.

### Where are the requirements for transient suppression?

A bypass capacitor in parallel with the TVS helps protect the PoE system from damage caused by transients. The TVS should be selected so it does not activate below the 57-V maximum required application voltage but activates before reaching the 68-V absolute maximum rating.

### How can a designer configure a PoE system?

ICs available from several manufacturers simplify PoE system design. These ICs usually include an IEEE 802.3af-compliant interface for PDs and a dc-dc converter.

### What system elements offer fault protection?

First, the PSE may remove power from a PD that is either violating its power class or the maximum current draw level of 400 mA. Second, the PD interface IC may have both internal current limit and thermal limit protection. Finally, the chosen power-supply controller may have cycle-by-cycle current limit protection as well. Different ICs offer different levels of protection.

ED Online 9076

**New! Power-over-Ethernet Online Seminar**  
**For free online design tools, samples, evaluation boards,**  
**datasheets and more visit:**  
**power.national.com**